AMENDMENTS TO THE SPECIFICATION

Please amend paragraph [0044] as follows:

[0044] Figure 6 illustrates a schematic block diagram of the duty cycle distortion correction module 88. In this embodiment, the duty cycle distortion correction module 88 includes a plurality of inverters 100-106 and correction blocks 108 and 110. As shown, inverter 100 receives clock while inverter 104 receives clock bar. The outputs of inverters 100 and 104 are provided to the serial-to-parallel converters 44 and 46 of the serial-to-parallel conversion module 18. In addition, the outputs of inverters 100 and 104 are provided to inverters 102 and 106, respectively. To compensate for duty cycle variances, correction blocks 108 and 110 are coupled in parallel with inverters 102 and 106. Each correction block includes the circuitry illustrated in the correction block ~~108~~ 110 coupled in parallel with inverter 106.

Please amend paragraph [0064] as follows:

[0064] As one of average skill in the art will appreciate, the number of steps in changing the gain may be more or less than the number shown and the switches of the gain network may be transistors, gates, et cetera. In addition, one of average skill in the art will appreciate, other embodiments for producing the programmable gain network 254 ~~154~~, logic 256 and corresponding inputs to the logic 256 may be readily derived based on the desired functionality of the offset module 181 and the description provided herein.